

Process Transferability from a Spot Beam to a Ribbon Beam Implanter: CMOS Device Matching

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Abstract. The exercise of dose and energy matching is the standard way to integrate a new implanter into a manufacturing fab. Sheet resistance and secondary-ion mass spectroscopy (SIMS) measurements on bare silicon wafers have been the conventional metrologies to establish dose/energy equivalence between implanters. Invariably, matched performance on bare silicon wafers translated into matched device performance between implanters of the same kind. However, as devices scale down to 90 nm and beyond, the implanter design can become a significant factor in terms of process matching. In this paper we discuss the dynamics of transferring 120-90nm logic processes from a traditional batch, spot beam implanter to a single wafer (SW), parallel ribbon beam implanter. The results show that the traditional approach to dose matching involving the basic parameters of specie, dose and energy, although necessary, is inadequate to provide matched device performance between the two implanter types. 3-dimensional effects which cannot be represented by bare silicon wafers necessitate the use of device wafers to meet the target requirements.

Keywords: Ion Implantation; Batch implanter; Single wafer implanter; Spot beam; Ribbon beam

PACS: 61.72.Tt, 85.40.Ry

INTRODUCTION

Spot beam batch tools have been the traditional workhorse for high current implanters for more than 2 decades. In the past several years, due to the increased sensitivity of devices to critical factors such as defects, beam angle, contamination and productivity etc, the need for single wafer (SW) high current implanters has become more and more important. Parallel ribbon beam, single wafer implanter is one of the approaches to meet these needs. This tool delivers a parallel and uniform beam across the wafer and requires only vertical mechanical scanning of the wafer. Since many companies had developed their devices on batch implanters, the switch to SW tool requires meticulous understanding of the device effects especially as dimensions scale down to 90 nm and beyond.

In this paper, we present process matching results from a traditional batch implanter to a SW ribbon beam implanter. The paper will focus on 120 and 90nm logic devices, on which interesting results have

been observed concerning angle control, energy purity and dose rate effects.

EFFECTS OF ANGLE CONTROL RIBBON VERSUS SPOT BEAM

Beam blow up due to space charge effects is a well known phenomenon in ion beam transport. These effects are more significant at lower energies. Consequently, in a self aligned implant such as source drain extension (SDE), a blown up beam leads to dose loss at the edges due to shadowing of the beam caused by the gate electrode. Devices developed on a tool with spot beam architecture inherently exhibited this behavior although such effects went unnoticed until recently when the parallel ribbon beam ion implanter was developed. It is in the transfer of processes between these two tool types, when such effects become very evident. The phenomenon of dose loss due to shadowing by the gate is best illustrated in Figure 1. A controlled, parallel beam delivers the desired dose at the edges of the gate-offset spacer

whereas a dispersed spot beam leads to loss of dose and encroachment under the spacer. Transferring a SDE process from spot beam to the parallel beam case would intuitively imply that the latter would have to lower the dose to match transistor characteristics.

Previous investigations [1] with 130nm NMOS devices have demonstrated that the As⁺ SDE dose on the parallel ribbon implanter had to be lowered by ~ 22% to achieve matched transistor performance between the two tool types.

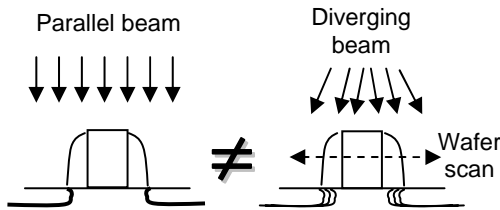


FIGURE 1. Different dopant interactions around spacer edge on parallel ribbon beam versus spot beam

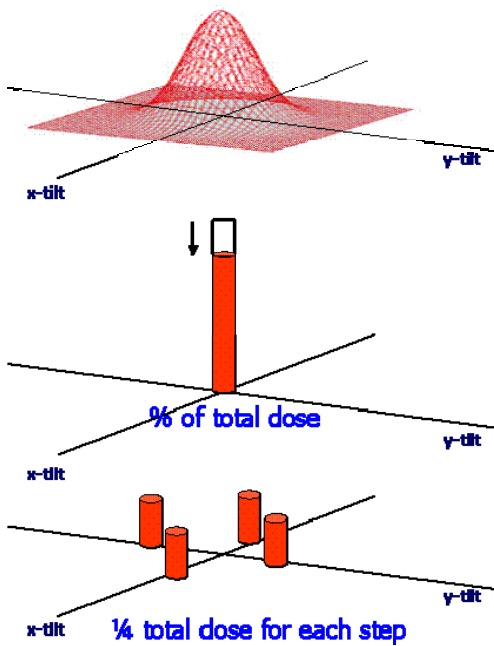


FIGURE 2. (a) Illustration of a spot beam, (b) parallel ribbon beam mimicking a spot divergent beam by dose reduction for 0° and (c) by low tilt quad implant

This paper discusses the transfer of a self-aligned SDE process for a 90nm logic device from the spot beam batch implanter to the single wafer, parallel ribbon beam implanter. Two approaches to match the transistor performance were investigated – (i) lowering

the dose on the ribbon beam tool with 0° tilt to mimic previous investigations [1] and (ii) low tilt angle quad mode to mimic the dispersion effects of the spot beam. Both approaches are illustrated in Figure 2.

90nm p-SDE matching

The SDE implant for 90nm PMOS is a BF₂, 2keV, mid E14 cm⁻² implant. The actual dose used is proprietary. As usual, traditional R_s and SIMS analysis was done to match the tools as closely in dose and depth as possible. TCAD simulation using the device parameters was also done to provide guidance on the dose skew that should be employed to define the correct dose scalar which would lead to matched device performance between the tools. Based on the results of this pre-work, the dose was skewed from 90% to 75% of the dose matched with R_s and SIMS. Drive current (I_{dsat}), threshold voltage (V_t) and R_s (Poly) were compared. The I_{dsat} results from the various dose skews and tilt tests are depicted in Figure 3. Due to space limitations of the paper, only the I_{dsat} results have been included. Mean value is represented by the diamond box while the other symbols are standard: data distribution is represented by a box plot that contains 25 to 75% of the distribution and other bars show the following limits: 0%, 10%, 90% and 100%.

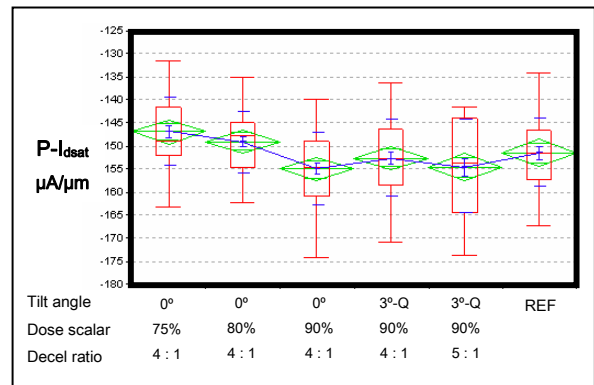


FIGURE 3. I_{dsat} as a function of various SDE implant conditions including dose skew, tilt angle and decel ratio

All dose skew tests were done with 0° tilt. The effect of changing dose on the ribbon beam tool is strongly evident in the first 3 data sets from the left where the dose was varied from 75% to 90%. This data shows that near perfect matching of the I_{dsat} is achieved with a dose scalar setting of ~ 85%. This result is consistent with previous observations although the exact dose required for matching is

different depending upon the device design and other factors.

The 4th data set from the left shows that a 3° tilt quad mode implant, with almost equivalent dose to the reference tool also provides adequate matching. The choice of which one to adopt is up to the user, but these results demonstrate that there are multiple options with a controlled, parallel ribbon beam to mimic the performance of a spot beam tool. Such effects would not be evident if only bare silicon wafers were employed in process matching of tools. This is further evident in the P-SD tests described later.

Effects of Energy Contamination

It is to be noted that the aforementioned tests for the p-SDE were done in decel mode on the ribbon beam tool, whereas the reference tool runs the same implant in a drift mode. Preliminary work, although not included here due to space limitations showed that a decel ratio of 5:1 and higher, skewed the I_{dsat} results. This is reflected in the 5th data set from the left in Figure 3. This is due to the increased energy contamination (EC) stemming from high decel ratios. Previous work [2] has shown that skew in drive current and V_t resulting from EC in SDE implants can be recovered by adjusting the dose of the halo implant. However, we did not choose to take this approach. Instead, maintaining a decel ratio of 4:1 was adequate for device and production applications.

90nm p-SD matching

The 90nm PMOS source drain (p-SD) implant is a 0°, 2 keV Boron implant with mid $E15cm^{-2}$ dose. Both tools employ decel mode operation for this implant.

As was the case with p-SDE, traditional R_s and SIMS with bare silicon wafers was used to achieve the first order matching between tools. SIMS profiles from the annealed samples on both tools are presented in Figure 4 and show that despite the higher decel ratio on the ribbon beam tool than the reference tool, no difference in the depth profiles is observed.

Based on R_s and SIMS results, the first split lot was run with a dose scalar of 114%. Results showed that $p-I_{dsat}$ was 7% higher than the reference tool. Correspondingly, active and polysilicon resistances measured on devices were lower by 7%. These results would indicate that the ribbon beam implanter was overdosing relative to the reference spot beam tool.

Subsequently, another device split was performed, whereby the dose was reduced by 5% and 10% on the ribbon beam tool. In addition, to mimic the spot beam

characteristics, a 3° tilt test was also performed in quad mode as was done in the p-SDE case described earlier.

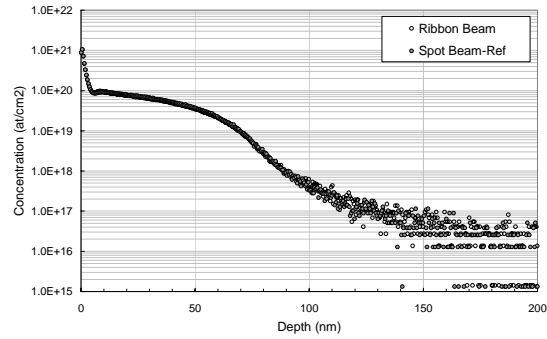


FIGURE 4. Matched dopant depth profiles for 90nm p-SD implant (B^+ , 2keV) after spike anneal

Table I summarizes the key device parameters from these tests.

TABLE 1. Main PT results of 90 nm pSD split lot

Split conditions	PI_{dsat} ($\mu A/\mu m$)	V_t (mV)	Poly R_s (Ω/sq)
Batch tool (reference)	-173.8	-499.0	445.2
SW 109% trim – 0° tilt	-172.8	-501.4	436.3
SW 104% trim – 0° tilt	-163.8	-509.0	449.6
SW 104% trim – 3° tilt	-167.8	-506.6	452.2

Results show that dose adjustment alone is not adequate to match all device parameters. Indeed, the 0° tilt approach would require a dose scalar $\sim 109\%$, but polysilicon resistances are not matched for devices of different sizes. The combination of lowering the dose scalar to 106% with a 3° tilt provides the best matching conditions. In essence, the effect of tilting the wafer by 3° on the ribbon beam implanter is to increase I_{dsat} by $4\mu A/\mu m$, which is equivalent to a 2% increase in dose. This is attributed to having a higher concentration of the dopant under the spacer.

DOSE RATE EFFECTS

120nm P-SD matching

This section discusses the preliminary findings from tests conducted to match the p-SD process between the tools for a 120nm logic device. The implant in question is a 15 keV, BF_2 beam at 7° tilt with a dose in the mid $E15cm^{-2}$ range. Again, the exact dose is not mentioned due to proprietary considerations.

Same methodology as for 90nm was used for the process matching of this recipe on bare silicon. A dose trim of 100% was found to match both R_s and as-implanted depth profiles.

Based on these results, a first device split was performed with a dose trim at 100% on the ribbon beam tool. Results are summarized in Table II.

Table II. Mean values of device parameters (120nm)

Split conditions	$P I_{dsat}$ ($\mu A/\mu m$)	P+ Active R_s (Ω/sq)	P+ Poly R_s (Ω/sq)
Spot beam tool (ref)	-284.7	129.0	330.8
Ribbon tool 100% Dose scalar	-280.0	121.4	325.0

First results show that the 120nm devices processed on the ribbon beam tool exhibit lower I_{dsat} by $\sim 5 \mu A/\mu m$ compared to reference devices. Associated P+ poly resistance and active resistance values were lower by ~ 6 and $\sim 8 \Omega/sq$ respectively. Relative to the reference devices, shift in Poly resistance can be explained by a 2~3% overdosing on ribbon beam implanter, however the $8 \Omega/sq$ shift in active resistance can not be explained by a simple dose change. Indeed, based on our experience, a 10% change in dose changed this parameter only by $\sim 3 \Omega/sq$.

These apparently contradictory results (lower resistances, but lower I_{dsat}) led us to run another device split with different implant conditions on the ribbon beam tool. Dose scalar was reduced by 3% to match P+ polysilicon resistance. To investigate the I_{dsat} behavior, different conditions were tested – (i) lowering the dose rate by reducing beam current from 13mA to 3mA, (ii) reduce the decel ratio for the implant and (iii) increase tilt angle from 7° to 10° (same concept as used on 90nm p-SDE). Results are summarized in Table III.

Table III. Results of second 120nm pSD device split

Split conditions	$p-I_{dsat}$ ($\mu A/\mu m$)	P+ active R_s (Ω/sq)	P+ Poly R_s (Ω/sq)
Ref tool	-286.3	127.3	325.2
7° tilt - 13 mA	-280.0	120.5	324.4
10° tilt - 13 mA	-278.0	122.1	325.0
7° tilt - 3mA	-284.9	122.0	322.8
7° tilt - Lower decel ratio	-285.2	120.6	324.1

It is observed that with 3% dose reduction, poly resistance is better matched to the reference regardless of the implant conditions. As expected, I_{dsat} is still lower by $\sim 6 \mu A/\mu m$ for the standard implant conditions (7° tilt, 13mA). In addition, increasing the tilt angle from 7° to 10° did not have any impact on the results. This is expected as the SD implant is isolated from the gate edges by the spacer. Interestingly enough, lowering the beam current and reducing the decel ratio both resulted in I_{dsat} values closely matched to the reference value. These results indicate that dose rate is probably the key factor for this implant level. However, the P+ active resistance still shows a mismatch. The behavior of defects and activation as a function of dose rate has been more rigorously investigated by our co-workers and will be published in these proceedings [3]. Indeed, the results of this work show that the density of defects in the spot beam case is higher. Consequently, after anneal, a higher fraction of the Boron is trapped in the defect region and is not substitutional. We hope that tuning the beam with a lower density will enable the matching of both parameters. This is the focus of our future investigations.

CONCLUSIONS

With devices becoming increasingly sensitive beyond the 90nm node, traditional dose matching methods involving TW, R_s and SIMS measurements on bare silicon wafers are no longer adequate. This paper demonstrates that, to fully consider the impact of angle, energy purity and others effects such as dose rate, findings on bare silicon wafers must be validated through device measurements and appropriate adjustments must be made before releasing the process to production.

REFERENCES

1. U. Jeong, S. Mehta, C. Campbell, Z. Zhao et.al, "Effects of Beam Incident Angle Control on NMOS S/D Extension Applications," 14th International Conference on Ion Implantation Technology, 2002, pp. 64-68
2. U. Jeong, S. Mehta, G. Li and J. Liu, "Energy Contamination in Low Energy Implantation," Semiconductor International, October 2003
3. N. Cagnat, C. Laviron, N. Auriac, J. Liu, S. Mehta, L. Frioulaud & D. Mathiot, "Defect Behavior in BF_2 Implants for S/D Applications as a Function of Ion beam Characteristics," These proceedings.