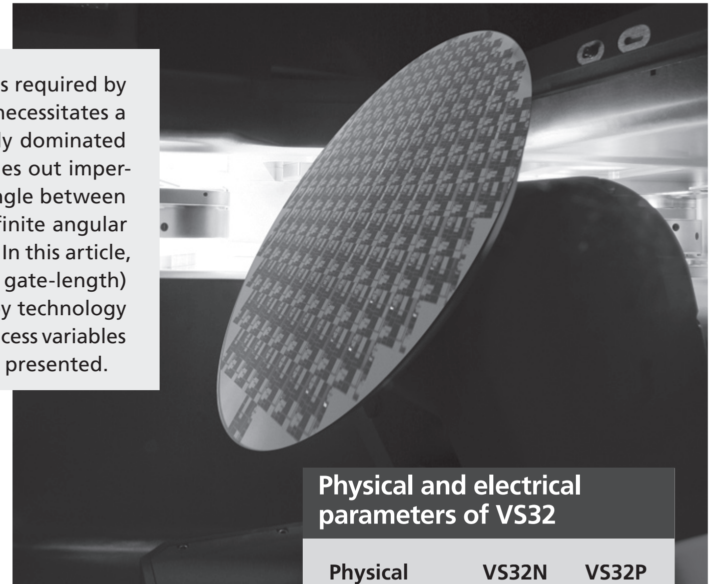
Precision requirements for advanced HP logic implantation

EXECUTIVE OVERVIEW The decrease of junction depths required by device scaling implies a shrinking thermal budget that ultimately necessitates a "diffusion-less" anneal. The final dopant distribution is increasingly dominated by the as-implanted dopant profile, as diffusion no longer averages out imperfections in the implant. Such imperfections may include a finite angle between intended and actual angle of incidence as seen by a device, or a finite angular spread of the beam, collectively referred to as "implant precision." In this article, implant precision requirements for 32nm half-pitch (25nm physical gate-length) high-performance (HP) logic are reviewed; effects are analyzed by technology computer aided design (TCAD) simulations; and a Pareto chart of process variables along with their impact on a transistor's saturation current (I_{dsat}) is presented.



Traditionally, an implant process is defined by the implant species' atomic mass, energy, dose, and angular wafer positioning with respect to the projected beam direction (beamline axis). For device generations >0.18µm, simply meeting junction depth (x_j) and sheet resistance (R_s) targets for source/drain-extensions (SDE) junctions would virtually guarantee meeting target device characteristics. But today, this is no longer the case, and process variables such as the angular properties of the beam need to be taken into account. These additional requirements can be described comprehensively by three parameters:

- **Global steering angle** (wafer-to-wafer mean angle): The time average over all ion trajectories at a given point on the wafer followed by the spatial average over all points on the wafer. Certain implant tools have the capability to zero this angle out.
- **Local steering angle** (within-wafer angular spread): The time average over all ion trajectories at a given point on the wafer. This parameter will, in general, vary across the wafer (local steering angle variation).
- **Angular spread** (within-device angular spread): The width of the distribution of individual ion trajectories impinging on a fixed point on the wafer.

VS32: a virtual 32nm technology

To investigate the impact on electrical device parameters, we used TCAD simulations of 32nm half-pitch HP transistors. We designed a virtual technology, optimized with respect to I_{dsat}, I_{off}, subthreshold slope, *S*, and drain-induced barrier lowering (DIBL). The main technology elements were extrapolated from published 65nm and 45nm HP technologies. Specifically, we use a physical gate length of 25nm, a physical gate-oxide thickness of 1.1nm (corresponding to an electrical gate-oxide thickness in inversion of 1.6nm), offset-spacers of 6nm length, embedded source/drain-SiGe (eSiGe) and stress layers, dopant activation with negligible diffusion (e.g., Flash or LTP), and NiSi contacts. We note that the gate length and gate-oxide thickness differ significantly from the ITRS 2005 prediction [1], but are in line with industry trends. Selected electrical device parameters are shown in the **table**.

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Physical and electrical parameters of VS32

Physical	VS32N	VS32P
Overlap (nm)	1.9	3.4
x_j^{ext} (nm)	13.7	11.5
x_j^{SD} (nm)	32.2	42.6
Electrical		
V_{dd} (V)	1.1	1.1
I_{dsat} (mA/µm (n/p))	1.79	1.07
I_{off} (nA/µm)	146	165
DIBL (mV/V)	167	191
S (mV/dec)	90	95.2
V_{th}(V)	0.32	–0.29
C_{gs} aF/µm	273	286
f_t (GHz)	494	370
τ (ps) (n/p)	0.32	0.43

Local steering error

In the design of an advanced device technology, a large fraction of the extension dopant profile is contributed by the as-implanted dopant profile, as opposed to diffusion. Even small local-beam steering angles, θ_{local}, during the extension implant lead to significant changes in the device performance. As **Fig. 1** shows, for the nFET, as little as a 1° θ_{local} leads to a reduction of 3% in I_{dsat}.

Source-side shadowing ($\theta_{local} < 0°$), i.e., a decrease in the source-extension doping, leads to more severe I_{dsat} degradation than drain-side shadowing. For I_{dsat}, therefore, it is confirmed that the source-side overlap, and hence the source-side resistivity of the extension, is far more important than the drain-side overlap and extension resistance [2].

In a manufacturing environment, non-zero local steering angles appear as a non-zero asymmetry, or device-skew, during wafer-electrical-test. I_{dsat} is first measured in the normal way, and then it is measured as I^r_{dsat} with source and drain probing voltages exchanged. The skew is then defined as $2(I_{dsat} - I^r_{dsat})/(I_{dsat} + I^r_{dsat})$. For the VS32 nFET, the skew is shown in Fig. 1. Other DC and AC device parameters, such as threshold voltage or transit frequency, are impacted in a similar way. Qualitatively the same is true for the pFET DC and AC device parameters. However, for both pFETs and nFETs, the magnitude of the effects depends on the device design.

The effect of local beam steering during the nSDE (n-type source-

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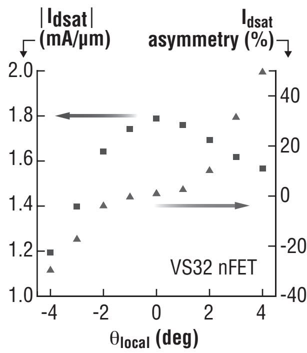

Figure 1. I_{dsat} (blue squares) and its skew (red triangles) as a function of local steering angle, θ_{local}. Source-side shadowing corresponds to θ_{local} <0°.

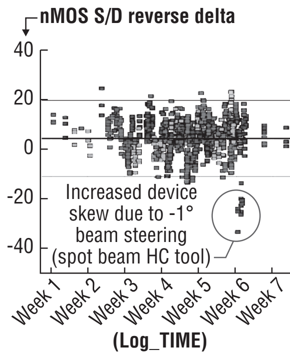

Figure 2. Production SPC 90nm nMOS device skew chart with As SDE implant performed using four different high current tools.

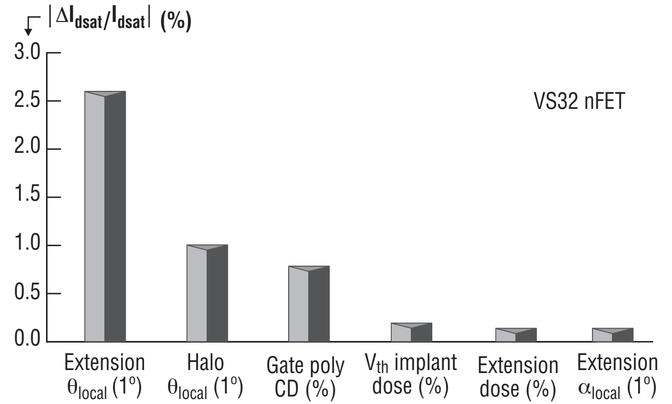

Figure 5. Pareto chart for I_{dsat}.

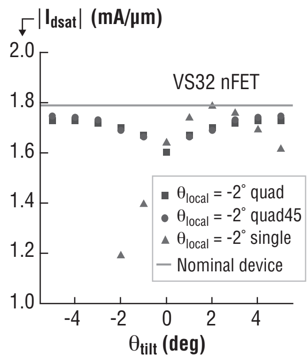

Figure 3. I_{dsat} for a single (green triangles), a quad (blue squares), and a quad45 (red circles) implant, as a function of tilt angle, all for a local steering angle of –2° (source-side shadowing).

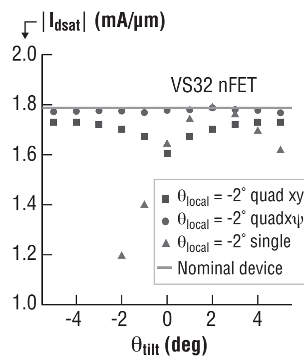

Figure 4. I_{dsat} for a single (green triangles), a quad (blue squares), and a quad45 (red circles) implant, as a function of tilt angle, all for a local steering angle of –2° (source-side shadowing).

drain extension) implant in single mode on device skew in a high-volume manufacturing environment is illustrated in **Fig. 2**. Device lots produced using one of the tools (squares) show skew values outside of the allowed process control limits. Vertical beam steering ranging from 0.75° to 1° has been identified as a root cause of the increased device skew and corresponding yield loss.

Mitigation of local beam steering

Quad implants, where a quarter of the dose is implanted at a fixed tilt-angle and azimuthal rotations of 0°, 90°, 180°, and 270°, reduce the impact of beam-steering (**Fig. 3**). Figure 3 compares I_{dsat} as a function of tilt-angle for a beam steering angle of –2° (source-side shadowing). A dramatic improvement is seen for a quad implant (blue squares), provided the tilt angle is sufficiently large. Even better is a "quad45" (red circles), where the rotations are 45°, 135°, 225°, and 315°. Still, even in the best case, I_{dsat} is reduced by ~2%.

Influence of endstation type

Implanter endstations come in two configurations, depending on whether the twist is produced by 1) tilts around two orthogonal axes ("xy"), or by 2) a rotation around the wafer normal ("xψ"). The latter configuration is superior in mitigating local beam steering with a quad, as **Fig. 4** demonstrates. A quad on a xψ-endstation mitigates the effect of the –2° beam steering to within 0.5%; in fact, it does this even at a tilt of 0°, in contrast to the xy-endstation. This mitigation occurs because for a xψ-endstation at zero tilt, the device still sees the steering angle as an "effective tilt angle" around which a quad-mode rotation is possible. The xy-endstation, on the other hand, is incapable of producing a rotation at zero tilt.

Pareto chart

The impact of various process variables on I_{dsat} of the nFET in VS32 is compared with that from the extension implant local steering angle in **Fig. 5**. We see that the implant angle precision is the most important parameter to control to achieve high yield.

Conclusion

For 32nm half-pitch and beyond devices, a large fraction of the final dopant profile is contributed by the as-implanted dopant profile, as opposed to the contribution by diffusion. As a consequence, small changes in the as-implanted profile from the desired one are beginning to have a disproportionate impact on device characteristics.

For the 32nm half-pitch nFET discussed in this article, as little as 1° of beam steering angle during the extension implant leads to a reduction of 3% in I_{dsat}. Extension beam steering is the largest contributor to I_{dsat} degradation, ahead of halo implant beam steering, gate-poly CD variations, or implant dose. It is therefore imperative that beam steering and beam parallelism are well controlled to achieve high yield in the production of advanced HP technology. Implanters that fulfill these requirements are available. The angle control elements of the VIISta HCP single-wafer, high-current implanter ensure that beam steering and beam parallelism are measured, controlled, and interlocked prior to each implant with a repeatability performance of <0.1°. The impact of beam steering in device performance can be alleviated significantly by a quad implant—and this mitigation is superior for an end-station that accomplishes the wafer rotation during a quad by an actual rotation. ■

References

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2. T. Ghani, K. Mistry, P. Packan, M. Armstrong, S. Thompson, S. Tyagi, M. Bohr, "Asymmetric Source/Drain Extension Transistor Structure for High-performance Sub-50nm Gate Length CMOS Devices," paper # T3-A1, *2001 Symp VLSI Technol. Digest Tech. Papers,* IEEE, New York, NY, US, 2001.

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